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PRINCIPLE DESIGN OF 300 KHZ MECO RF KICKER BIPOLAR SOLID STATE MODULATOR*

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Abstract

A high speed, high repetition rate, bipolar solid-state high voltage modulator is under development at Brookhaven National Laboratory for Muon Electron Conversion (MECO) Experiment. The modulator will be used to drive a RF kicker consisting a pair of parallel deflecting plates. The principle design is based on the inductive-adder topology. This system requires a fast pulse rise and fall time about 20ns, a pulse width of 100ns, a pulse repetition rate of 300 kHz, and a 60 kHz sine-wave amplitude modulation. The fast high voltage MOSFETs are used as main switching devices. Different magnetic materials are being investigated for adder core magnets. The main circuit design, critical subsystems, and major technical issues will be discussed. The circuit simulation, components selection and evaluation, and preliminary test results will be presented.

I. INTRODUCTION

In recent years, the successful development of ultra-fast high voltage pulse modulators with the inductive adder technology has attracted wide attentions [1]. Together with the advancement in solid-state switching devices and nanocrystalline magnetic materials, its application is becoming more and more popular. The principle design presented in this paper is motivated by the inductive adder digital modulation method demonstrated in [2].

The basic requirement of the MECO RF kicker modulator is given in Table I and illustrated in Figure 1.

Table I: Main Parameter specifications.

Output Voltage	± 4000 V
Peak Output Current	± 40 A
Load Impedance	100 ohm
Pulse Repetition Rate	300 kHz
Pulse Rise Time	20 ns
Pulse Fall Time	20 ns
Pulse Flat Top	100 ns
Output voltage Modulation Frequency	60 kHz
Output Voltage Modulation Waveform	Sinusoidal
Number of Pulse per Modulation Frequency Period	5

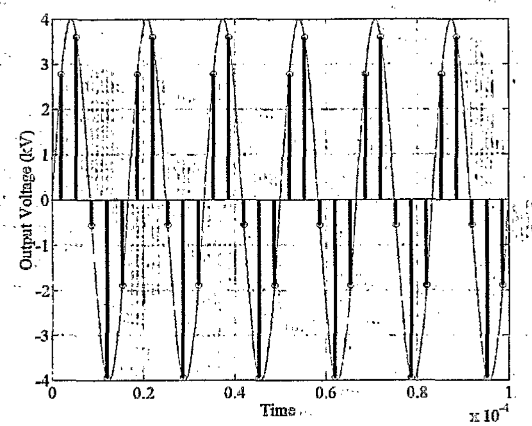

Figure 1. Bipolar pulse output at 300 k Pulse-Per-Second with 60 kHz modulation.

In this specification, the output amplitude has a sine wave RF modulation of 60 kHz, and the output pulse has a repetition rate of 300,000 pulses per second. The output pulse shall be trapezoidal shape with a 20 ns rise time and fall time, and a 100 ns pulse flattop. The intra-pulse duration is 3.193 µs. The output pulse polarity and amplitude will change on a pulse-to-pulse basis.

II. DESIGN PRINCIPLE

Assuming a multi-cell inductive adder, each cell drive circuit is charged to the same or different voltage level. A different combination of discharges from selected cell drive circuits will generate different output pulse. Let Vmax be the maximum output voltage, V1 be the maximum voltage per cell diver circuit, then the number of cell required is

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$$N = \frac{V\max}{V1}. \quad (1)$$

Here the resolution of output voltage is V1. For better amplitude resolution, trimming cells with partial voltage can be added. If V2 is one- half of V1, V3 is a quarter of V1, and V4 is one eighth of V1, and so on, we have

$$Vi = \frac{V1}{2^{i-1}}. \quad (2)$$

The lowest charging level will define the resolution of the output voltage.
Since

$$\sum_{i=2\to\infty} \frac{V1}{2^{i-1}} = V1 \quad (3)$$

the number of cells required with drive voltage V1 can be reduced to N-1.

To obtain bipolar pulse output, each adder cell will have both positive windings and negative windings. Using wire windings will result large leakage inductance and distort adder property. Therefore, we will use slotted primary windings. This can be done with top and bottom plates slotted, and the central cylinder kept integral.

The positive adder cell drive boards will be connected as usual, and the negative adder cell drive boards will be mounted upside-down. The triggers and controls can then be kept at ground level. The positive adder cell boards and negative adder cell drive boards will be arranged in an interleaf fashion to distribute current evenly around adder core.

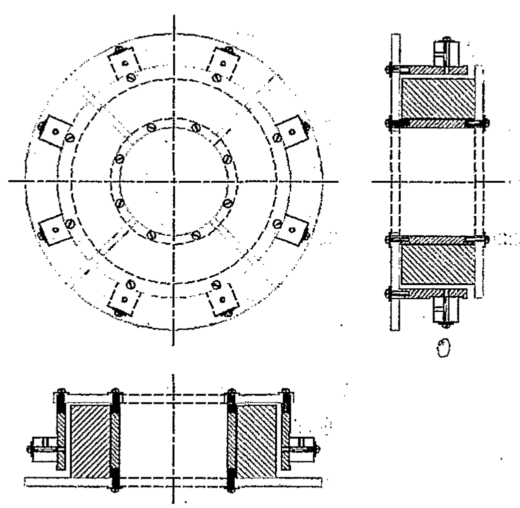

Figure 2. Split primary winding for bipolar output pulse.

The adder stalk can have unidirectional or bi-directional output. We have options to use two unidirectional stalks each with ± 2kV output, or a bi-directional stalk of ±4 kV output. The load is a pair of parallel plates terminated with 50 ohm resisters, with plate-to-plate impedance of 100 ohm. Since voltage level in this design is not very high, it is better to use bi-directional output. The other advantage of using bi-directional output is that it requires only one set of lower voltage trimming cell for amplitude resolution, while two unidirectional adders will need double sets.

A M-stage bipolar inductive adder with bi-directional output is shown in Figure 3.

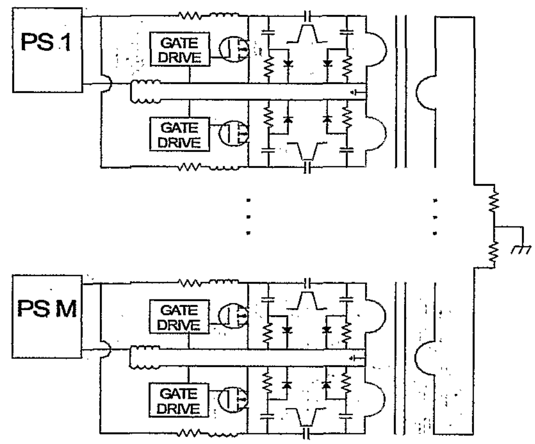

Figure 3. Principle diagram of a M-stage bipolar bi-directional output inductive adder.

III. DESIGN SIMULATION

Consider the specification of 4.0 kV maximum voltage here, if we limit the maximum charging voltage to 500 volts per cell drive, then the number of 500 volts drive shall be seven. In principle, with an additional five cell drives of 250 volts, 125 volts, 62.5 volts, 31.25 volts, and 15.625 volts each, one can achieve a resolution of less than 0.5% of maximum output voltage. The total number of adder cell in this design is twelve.

If the desired output pulses are located at angles of 18°, 90°, 162°, 234°, and 306° of a sine wave, then their amplitudes shall be 1.236 kV, 4.0 kV, 1.236 kV, -3.236 kV, and −3.236 kV, respectively. The graphical presentation is shown in Figure 4.

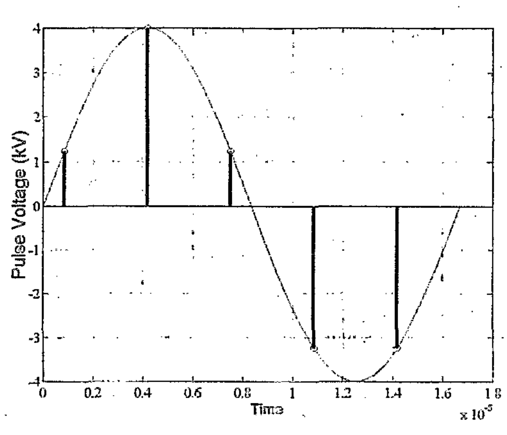

Figure 4. Waveform specification of design example.

To generate the required pulse pattern, one can selectively trigger the adder cell drive boards for each pulse as listed on Table II.

Table II. Trigger scheme of design example.

UNIT	Voltage	Pulse1	Pulse2	Pulse3	Pulse4	Pulse5
1	500	1	1	1	0	0
2	500	1	1	1	0	0
3	500	0	1	0	0	0
4	500	0	1	0	0	0
5	500	0	1	0	0	0
6	500	0	1	0	0	0
7	500	0	1	0	0	0
8	250	0	1	0	0	0
9	125	1	1	1	0	0
10	62.5	1	1	1	0	0
11	31.25	1	1	1	0	0
12	15.625	1	1	1	0	0
1	-500	0	0	0	1	1
2	-500	0	0	0	1	1
3	-500	0	0	0	1	1
4	-500	0	0	0	1	1
5	-500	0	0	0	1	1
6	-500	0	0	0	1	1
7	-500	0	0	0	0	0
8	-250	0	0	0	0	0
9	-125	0	0	0	1	1
10	-62.5	0	0	0	1	1
11	-31.25	0	0	0	1	1
12	-15.625	0	0	0	1	1
Output Voltage		1234.4	3984.4	1234.4	-3284.4	-3284.4

Adopting the circuit model used in reference [3], we expanded it to the bipolar pulse and bi-directional output configuration, as shown in figure 5. The parameters are estimated from the core material, core size, adder stalk size, dielectric insulation materials, and other circuit component parameters. Some assumptions were used to simplify the simulation, such as the ideal switching characteristics, low frequency primary inductance, etc. The snubber circuit and parameters are for illustration with ideal switch only; they are different from the actual circuit used in test.

The simulation results are shown in Figure 6 and figure 7. The upper trace and lower trace of Figure 6 are the current waveforms of positive plate and negative plate, respectively. The waveform shown in figure 7 is the voltage between positive plate and negative plate.

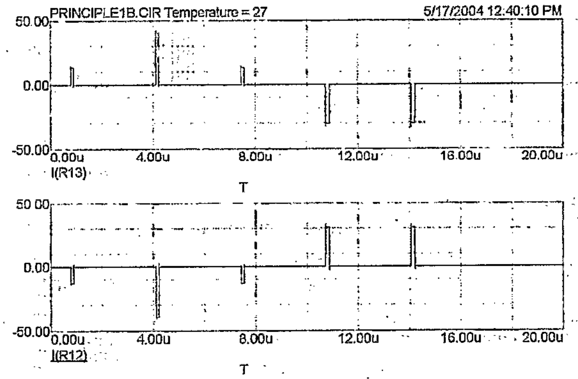

Figure 6. The upper trace is the current waveform of positive plate; and the lower trace is the current waveform of negative plate.

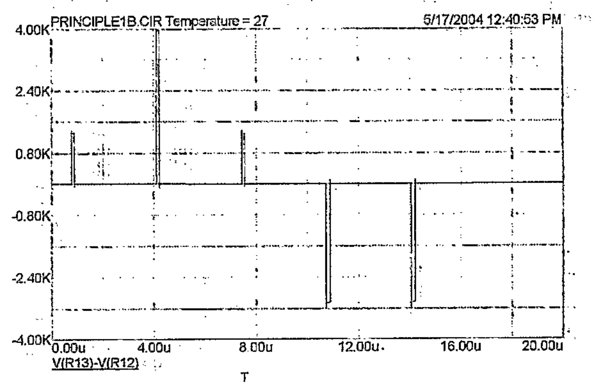

Figure 7. The voltage between positive and negative plates.

The above simulation demonstrates the design principle.

If a fixed pattern of output pulse is permissible, the number of adder cells might be reduced to simplify the system. Figure 8 is the simulated waveform of a nine cell adder with seven 500 volts and two 250 volts adder cells, which gives the similar result as in Figure 7.

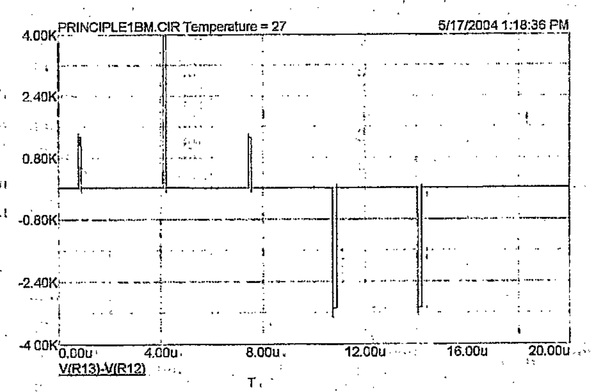

Figure 8. The voltage between positive and negative plates of the simplified nine-cell adder.

IV. DESIGN ISSUES

The critical components in this design are the adder cores, the switching MOSFETs, gate drives, high speed programmable trigger systems, and low inductance capacitors.

The main switch is IXYS RF Power MOSFET DE475-102N21A. It is rated for 1000 V drain to source, 24 A continuous and 144 A pulsed drain current at 25°C. This fast switch features 5 ns turn on time, 8 ns turn off time, and 5ns turn on delay. These make it ideal for this application. Two MOSFETs will be used for each positive or negative cell drives per adder cell. The applied voltage will be limited to 500 V for device reliability consideration. A total of 48 MOSFETs will be needed for the 12-cell bipolar pulser. The DEI EVIC420 gate driver and its evaluation board are used to drive the main switch. The test result is satisfactory. The Figure 9 is the switch and 1:2 core response test at 400 volts.

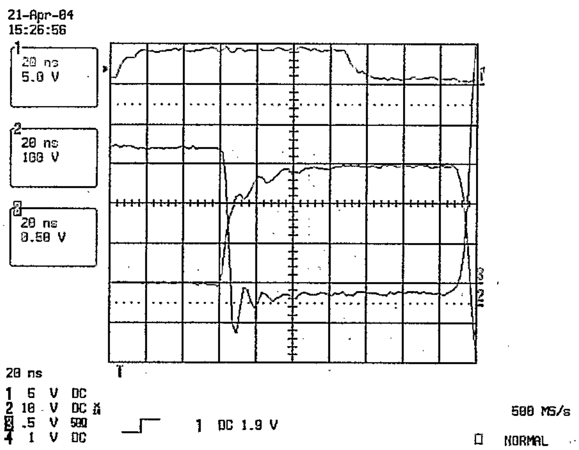

Figure 9. Upper trace is the input trigger, middle trace is the Drain to Source Voltage, and the lower trace is 1:2 core test response.

The capacitor used for test is WIPA MKP10 type, rated for 1000 V dc, or 600 V ac applications. Low inductance reconstitute mica capacitors will be considered for new assembly.

A soft ferrite core was used for initial test. The frequency response is very good, but the core loss is a big concern. The 300,000 pulse per second repetition rate operation with 20 ns rise and fall time will induce very high core loss. The METGLAS® and FINEMET® magnetic alloys are both being considered. A few NAMGLASS® 4 cased Toroids have been purchased for test. It is made of one mil thick FINEMET® ribbon. A short adder stalk is under design and assembly. The initial design is air-cooled. However, the actual core loss induced temperature rise will determine the cooling method for future assembly.

V. SUMMARY

In summary, the bipolar winding shall work in an ideal situation. However, the noise control of high voltage transient induced by the opposite winding during turn on and turn off is not an easy task. The lower voltage adder-cells may be much more sensitive to transient noise when operating with higher voltage cells. Also, the core loss is a serious issue in ultra-fast, continuous operation, high repetition rate inductive-adder systems.

VI. REFERENCES

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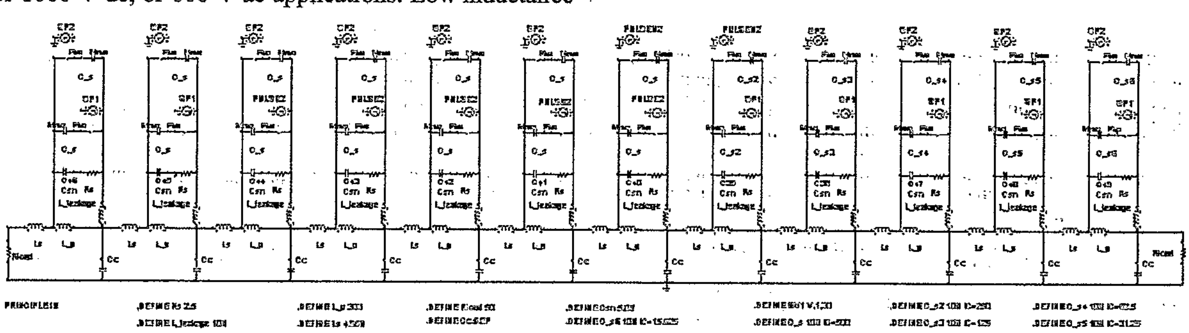

Figure 5. Simulation model of design example.