

DESIGN OF 2.4GHz CMOS DIRECT CONVERSION LNA & MIXER
COMBINATION FOR WIRELESS DATA-LINK TRANSCEIVER*

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(2000)

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Design of 2.4GHz CMOS Direct Conversion LNA & Mixer Combination for Wireless Data-link Transceiver

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Abstract: Three LNA and mixer combinations in $0.6\mu\text{m}$ and $0.4\mu\text{m}$ standard CMOS processes for direct-conversion receiver of 2.4GHz ISM band short-range wireless data-link applications are described in this paper. Taking low power dissipation as first consideration, these designs, employing differential common-source LNA and double balanced mixer architectures, achieve total conversion gain as high as 42.4dB, DSB noise figure as low as 9.5dB, output-referred IP3 as high as of 21.3dBm at about 4mA DC current consumption. This proves it is possible to apply standard CMOS process to implement receiver front-end with low power dissipation for this kind of application, but gain changeable LNA is needed to combat the dominant flicker noise of the mixer in order to achieve acceptable sensitivity and dynamic range at the same time.

I Introduction

With the introduction of 2.4GHz ISM band for custom wireless data-link applications, research on monolithic transceiver for different applications within this band is becoming hotter and hotter [1][2][3]. CMOS transceiver, due to its lowest cost among all possible processes and highest integration ability with digital baseband sub-system for eventual one-chip whole system solution, has come into being the focusing research point in this area [4]. LNA and Mixer, as two essential RF components of the of the receiver front end, when implemented by standard CMOS process normally used for digital circuits, suffer from limited analog/RF performance of MOSFET device as well as conductive substrate loss. This makes it difficult to implement CMOS LNA & Mixer with both high performance and low power dissipation features through current available processes. However, with the continuous scaling of CMOS process, this is becoming possible now [3], and will be in production in the near future.

As part of our study of monolithic CMOS transceiver for short-range low data rate application (60 feet link range, 256kbps bit-rate), we designed three LNA & mixer combinations using two standard $0.6\mu\text{m}$ and $0.4\mu\text{m}$ CMOS processes. We applied direct conversion architecture to minimize unavoidable off-chip components, therefore eliminate image-suppress filter between LNA and mixer, but meanwhile, make separate LNA and mixer evaluation impractical. Unlike other approaches that consider high performance as first priority [1][2][3][5][6][7][8], we take low power dissipation and small die area as our first consideration, as our application allows a loose specification for performances, such as a noise figure as high as 25dB. Since we considered some negative effects that are much worst in case of small device and low power during our design, we believe our approach would be expanded to wider applications in the future when device scaling makes adequate improvement on performances.

We designed and evaluated three LNA and mixer combination chips. The first one is based on a $0.6\mu\text{m}$ 3-metal-layer CMOS process that has special well for linear capacitor. We employed a PN junction varactor at the load of LNA to tune output frequency response. The second one is almost a scaled version of the first to fit a 3-metal-layer 2-poly-layer $0.4\mu\text{m}$ process. This one replaced varactor by a linear fixed capacitor made by two poly layers. The third one copied all designs from the second one, but modified the mixer to improve noise figure. Section II and III describe details of the LNA and mixer design respectively. Section IV covers layout design.

Section V gives measurement results as well as comparison with other available publications. Section VI concludes the whole paper.

II LNA Design

Gain, noise figure, linearity, input match and power dissipation are four major specifications of LNA. The former three trade with power dissipation, i.e. bias current. In order to achieve maxim performances at low bias current and acceptable input matching, we took several special steps during LNA design.

1) Topology Selection

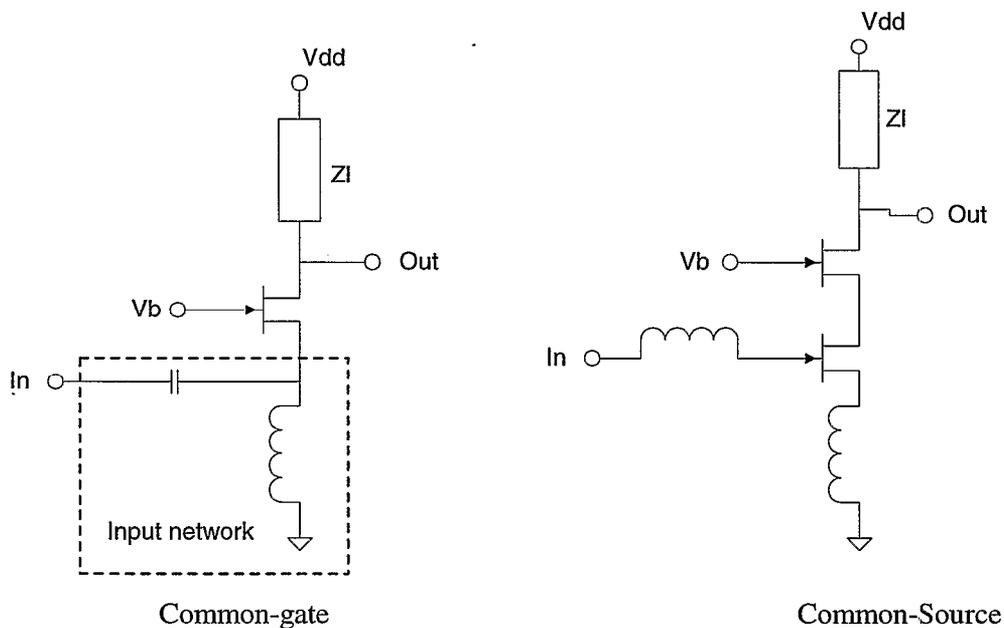


Figure 1 Common-gate and common-source LNA topology

Figure 1 shows two commonly used CMOS LNA topologies: common-gate and common-source. Common-gate applies the transconductance of the common-gate transistor as the resistance part of the input to match 50ohm source resistance directly or through a match network, while, common-source applies a degeneration inductance connecting the source of the common-source transistor to ground in order to generate a 50ohm real part input impedance and tune the imaginary part to zero by another series inductor connected to the gate. Table 1 lists simple calculation results of voltage gain and noise factor for these two topologies at perfect input matching condition.

Table 1 shows common-source is much better than common-gain in terms of both voltage-gain and Noise figure. As for linearity, since practical common-gain usually must employ negative resistance generation circuitry at the load to compensate its low gain, which ruins linearity, common-source is comparatively better. The drawback of common-source is poor input/output isolation, which is an important specification for direct conversion receiver. This is usually improved by cascode stage.

Table 1 Calculated voltage gain and noise factor for two LNA topologies

	Common-gate	Common-source
Voltage Gain	$\sqrt{g_m R_s} \frac{Z_l}{2R_s}$	$\frac{f_t Z_l}{f 2R_s}$
Noise Factor	$1 + \gamma + 4 \frac{R_s}{ Z_l }$	$1 + \gamma g_m R_s \left(\frac{f}{f_t} \right)^2 + 4 \frac{R_s}{ Z_l } \left(\frac{f}{f_t} \right)^2$

Note: g_m , R_s , Z_l are transconductance of the transistor, source impedance (50ohm), output impedance respectively.

g_m is generally chosen no more than $\frac{1}{R_s}$. γ is a noise index of the transistor, is 2/3 for long-channel MOSFET, but

could be 2-5 for currently used short-channel MOSFET. f and f_t are operating and transistor cut-off frequencies respectively.

Cascode common-source topology is selected for our LNA due to its overwhelming performance than common-gate especially under low bias current condition. 1mA bias current is chosen according to comprehensive consideration of transistor, input/output network and parasitics. In order to reduce parasitic effects caused by substrate coupling and second-order nonlinearity which is another important specification for direct conversion receiver, differential structure is adopted although it doubles power dissipation [9].

Noise factor equation of common-source topology in Table 1 seems to imply that the narrower the channel width is, the lower the noise figure could be. However, the present of gate resistance and gate induced noise that is included in more accurate noise model reveal that there is an optimal W/L ratio that gives lowest NF at an assigned power dissipation level [10]. W/L ratios of 150 and 100 are chosen in our design for main transistor and cascode transistor respectively.

2) Input-matching network

The input-matching network of an ideal common-source LNA contains two inductors connected to the source and the gate (shown in Figure 1), making source degeneration and resonance tuning respectively. Bias circuit and parasitics, however, complicate this issue. Input bonding pad is the dominant parasitic effect, which can be simply modeled as a series of capacitor and resistor (Figure 2). For a 100x100 μm^2 normal-size pad made above the P+ substrate, C is about 0.2pf, just a little smaller than the main transistor's input impedance, R is about 75ohm owing to conductive substrate.

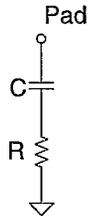


Figure 2 Equivalent circuit of bonding pad

Source degeneration inductor in our design is implemented by a 0.7nH 100x100 μm^2 on-chip spiral inductor with Q of 3, while resonance-tuning inductor is implemented partially by

bondwire, partially by off-chip component. In order to reduce parasitics' effects of to LNA's overall performance, a scaled pad is designed (see Section IV), which reduces C to about 0.08pF. Since this reduced parasitic capacitance still ruin the input match, an off-chip stunt capacitor is added, which turns off-chip matching components into L-shape network (see Figure 3). The designed prototype chip is directly glued and bonded on PCB. The off-chip inductor is implemented by thin short microstrip line.

3) Output network

One of the advantages of direct conversion architecture is that LNA is connected to mixer directly, no 50ohm interface needed. Therefore, according to equations in Table 1, the higher the output impedance is, the better performances are. This impedance is made of an on-chip spiral inductor connected to Vdd and a grounded capacitor (see Figure 3). In order to maintain small die area, the spiral inductor is design to occupy $168 \times 168 \mu m^2$ with a value of 8nH and Q of 4.5. The grounded capacitor is used to tune the resonant frequency of the network, making the impedance reach maxim value at the operating frequency. As we were not sure of the accuracy of the calculated inductance value, the first chip employs PN junction varactor as the tuning capacitor. The varactor's poor quality value is proven to pretty much ruin the whole performance. Fixed linear capacitor replaced it in the next two chips.

4) Overall schematic of the LNA

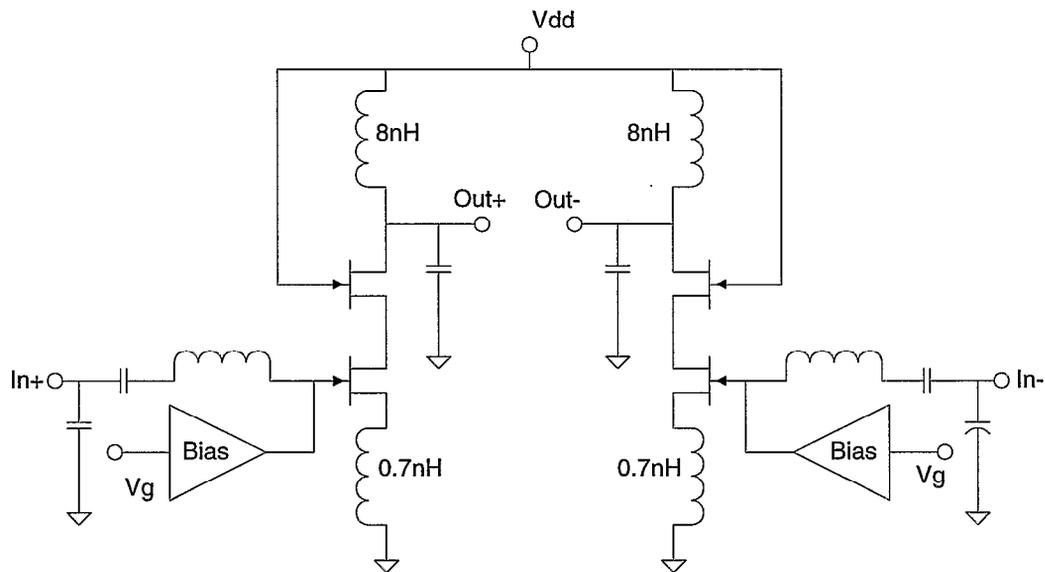


Figure 3 Schematic of the LNA

Figure 3 shows the overall schematic of the LNA. The bias circuit is designed to have about 10K output impedance, therefore comparatively ignorable in input matching.

II Mixer Design

1) Mixer topology

$$i_{flicker_noise}^2 = \frac{K_F I_{ds}}{C_{ox} L^2 f} \Delta f \quad (1)$$

It shows the noise output power is proportional to bias current. However, to reduce bias current is not a solution, because the power conversion gain is also proportional to bias current. Moreover, it makes the switches harder to turn on and off.

Our third chip is a special design to improve noise figure by all ways possible. In addition to the replacement of active load, it increases the channel width of all transistors and adds two current sources to the standard double balance mixer, as shown in Figure 5. On-chip source degeneration inductors are also used to improve linearity.

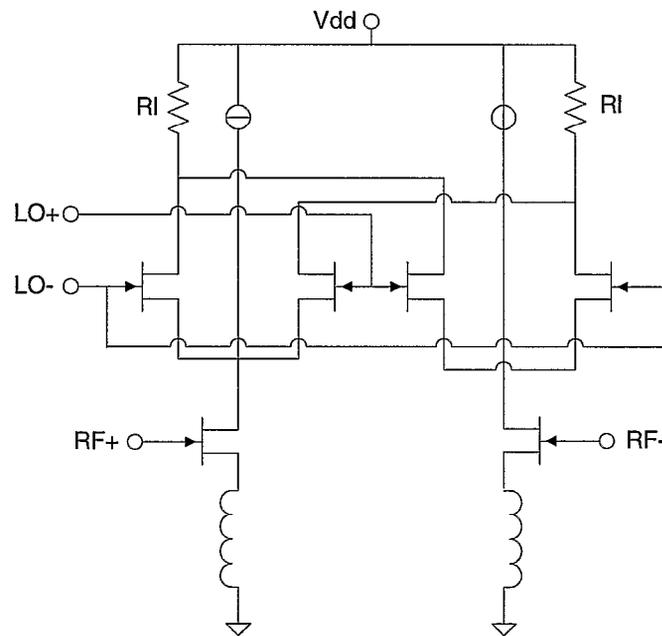


Figure 5 Modified double balance mixer

The increased channel width allows the two RF voltage/current conversion transistors to be biased at higher currents (1mA each), therefore increase the RF conversion gain and finally the total conversion gain. Meanwhile, the two current sources take the extra bias current, leaving the switches' currents unchanged, which means flicker noise output is unchanged. In order to reduce the current sources' influence to RF signal, the channel width of the switch transistors are also increased.

IV Chip Layout

The layout of CMOS RF circuits needs special care of the parasitic substrate coupling as well as parasitic resistance of all analog circuits. Every major transistor in the three chips is protected by wide substrate contact ring as close to the transistor as possible. This helps to reduce bulk resistance as well as coupling between transistors. In order to reduce gate resistors, all big transistors have 10 fingers, and fingers are connected from both sides. Considering the fact of wire bonding, the scaled RF pads are designed as octagon with only the top metal layer as surface, but rings of all-layer-stake at edge to enhance support. Grounded N well is located under it to shield substrate resistance. Thick rings of Vdd and ground are designed aside pads to reduce

resistance, except for RF input pads that needs to be close to the input transistor in order to reduce input resistor. The differential circuit is drawn as symmetric as possible. Figure 6 shows the layout of the third chip, which has a size of $1.2 \times 1.05 \text{mm}^2$.

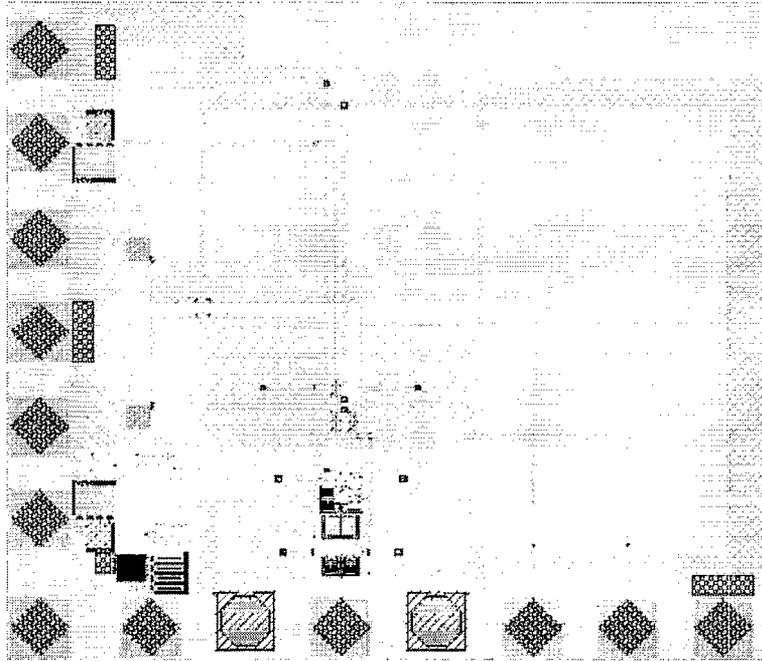


Figure 6 Layout of the third chip

V Measurement results

These three chips are directly glued and wire boned to the test board for measurement. In order to measure the differential structure by standard single-ended equipments, a microstrip balun is designed to convert RF input, and a differential amplifier with 0dB gain and 50ohm output impedance is connected to the IF output. The balun has a loss of only 0.7dB. The differential amplifier's output noise floor is at least 15dB lower than that of the whole circuit.

During every chip measurement, RF input impedance is first tuned with off-chip components to make S_{11} blow -12dB at the frequency of interest. Then, the total conversion gain and noise figure are measured with a setup of a spectrum analyzer, a noise source and ATE software. This setup is necessary because no available noise figure meter can test mixer with 128KHz IF. IP_3 is measured by a setup of two-tone test. Table 2 list test results of three chip with comparison with publications.

Table 2 shows Chip 1 and Chip 2 have similar IIP_3 . But Chip 2's conversion gain and NF are much better than Chip 1. These results are attributed by there factors: (1) Scaled channel length; (2) removal of the lossy varactor; (3) higher load impedance of Chip 2. The comparison between Chip2 and Chip3 shows, at the same process, higher RF gain brings lower NF, but lower IIP_3 owing to limited output dynamic range.

Behbahani *at. al.* reported a double-IF receiver in 0.6um CMOS for Wireless LAN applications [3]. Table 2 lists its results of LNA and first mixer. This is a heterodyne architecture. Conversion gain of the mixer is not reported. The much higher LNA bias current makes its LNA have better performances on gain, noise figure and linearity than our chips. The high IF frequency rules out flicker noise consideration, attributes to better noise figure for the mixer

Razavi reported another CMOS receiver for the 2.4GHz W-LAN application [2], which included test results for combination of LNA and mixer. His design includes single-ended common-source LNA, single-balance mixer and baseband amplifier with a gain of 10dB. The NF

and IIP3 in Table 2 is for the whole circuit, therefore is a little worse than those for LNA and mixer combination. (He expected a flicker noise corner of lower than 200kHz.) By comparing our chips to this design, we can see our chips have higher gain and similar output-referred IP3, but the flicker noise at lower IF limits NF and make us have to increase gain, which limits the input-referred IP3.

Table 2 Measurement results

	Chip 1	Chip 2	Chip 3	Behbahani <i>at. al.</i> 's[3]	Razavi's[2]	Meyer <i>at. al.</i> 's [1]
Process	0.6um CMOS	0.4um CMOS	0.4um CMOS	0.6um CMOS	0.6um CMOS	BiCMOS
Topology	Differential LNA, Double balanced mixer				Single-ended LNA, Single balanced mixer	Single-ended LNA, Double balanced mixer
IF	128KHz	128KHz	128KHz	190MHz	5.5MHz	350MHz
Current dissipation (mA) ¹	4	4.7	4	LNA: 8 Mixer: 3	LNA: 6 Mixer: 3	LNA: 4 Mixer: 8
Conversion Gain (dB)	27.1	38.5	42.4	(LNA: 29)	24	22 (LNA: 14, Mixer: 8)
NF(dB)	20.3 ²	11.6 ²	9.5 ²	2.5 (LNA: 2.4 Mixer: 15)	8.3 ²	3.3 (LNA: 2.2, Mixer: 11)
IIP3(dBm)	-16.9	-17.2	-23.7	LNA: 1.5 Mixer: 17	-9	LNA: -3 Mixer: +3
OIP3(dBm)	10.2	21.3	18.7	N/A	N/A	N/A

Note 1: The current dissipation of Chip 1~3 includes bias circuits. It also includes extra LO buffer in Chip 2.

Note 2: Due to direct conversion nature, these NF are DSB NF, which is 3dB low than test result.

Meyer *at. al.*'s s' BiCMOS approach[1] is also listed in Table 2 as a comparison. This design employs bipolar technology for LNA and mixer. Since it applies heterodyne architecture, measurement results of LNA and mixer are given separately. The bias currents are 4mA for LNA and 8mA for the mixer. Due to its bipolar feature, it achieves much better NF, but relatively worse IP3, at a cost of power dissipation even higher than Razavi's design.

VI Conclusion

Three CMOS LNA and mixer combination on two different processes for 2.4GHz ISM band short-range low data-rate application has been described. Through careful considerations for low power dissipation conditions, these designs achieved acceptable gain and noise figure and output IP3 at as low as 4mA total current bias. Due to their 128KHz IF, where MOSFET presents very

high flicker noise, extremely high gain is designed to combat the dominant flicker noise at the output port of the mixer, which limits the input IP3. With the scaling of the MOSFET channel length, this receiver front-end presents improvement of gain and noise figure. However, due to the dominant flicker noise that could even increase with the channel length scaling, the improvement of noise figure is limited.

These results show that it is possible to employ standard CMOS process to implement receiver front-end for 2.4GHz ISM band short-range low data-rate application at power dissipation even lower than that for conventional bipolar counterpart. In order to combat MOSFET's inherent flicker noise while maintain acceptable dynamic range, a gain changeable LNA is needed, which presents extremely high gain in case of weak input signal to achieve high sensitivity, but no gain in case of strong input signal to improve IIP3.

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