

## READOUT ELECTRONICS FOR A HIGH-RATE CSC DETECTOR\*

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## Abstract

A readout system for a high-rate muon Cathode Strip Chamber (CSC) is described. The system, planned for use in the forward region of the ATLAS muon spectrometer, uses two custom CMOS integrated circuits to achieve good position resolution at a flux of up to 2500 tracks/cm<sup>2</sup>/s.

## 1. THE ATLAS CSC SYSTEM

The CSC system forms the forward section of the muon spectrometer of ATLAS. It consists of 64 four-layer chambers of 768 x- and 96 y-strips. Interpolation is performed on the x-strips to achieve a resolution of about 50  $\mu\text{m}$  in the precision coordinate. Front end electronics cards are located around the perimeter of each chamber and enclosed by a Faraday shield. With 32 chambers per endcap the total channel count is 55,000. Fiber optic links transfer digital data, clock, and control signals to and from each chamber.

The acceptance of the CSC system is from  $2.1 < |\eta| < 2.7$ , resulting in an expected flux as shown in Fig. 2 (rates incorporate a standard "safety factor" of 5). Strips in the high- $\eta$  region will experience an average rate of about 600 kHz, taking into account the spread of charge on the cathode plane. Monte Carlo simulation shows that pileup effects can be tolerated if a bipolar pulse shape with a width less than about 1/5 of the average interpulse time is used.

Signals from each strip are amplified, filtered, and sampled at 40 Msa/s. Sampled data are stored on-chamber for the duration of the Level 1 trigger latency. To minimize the cost and power of the on-detector electronics, a switched-capacitor array (SCA) performs the sampling and storage in the analog domain. Upon receipt of a valid Level 1 trigger, the appropriate samples are read out, digitized, zero suppressed, and transmitted over fiber optic links to the read out drivers (RODs).

At a trigger rate of 100 kHz, and assuming ten 10-bit time samples to be read out per channel, per trigger, the gross digitization rate for the CSC system is  $6 \cdot 10^4 \text{ chan.} \times 10^5 \text{ Hz} \cdot 10\text{b} \cdot 10 \text{ samples} = 6 \cdot 10^{11} \text{ bits/s}$ .

Since chamber occupancy is of order 10%, simple zero suppression alone is not sufficient to reduce the data volume to a manageable level. It will also be necessary to suppress data belonging to out-of-time events, and to

track segments which do not project back towards the interaction point. Overall, a reduction of about  $8 \times \text{--} 20 \times$  is expected. The remaining data, about 1 Gbit/s per chamber, will be transmitted on optical fiber to the RODs, where space points will be extracted by interpolation.

## 2. SIGNAL PROCESSING

### 2.1 Pulse Shaping

Because we require a high SNR at high data rates, the signal processing is a tradeoff of rate-handling ability versus noise. By Monte Carlo analysis, it is found that the pileup effects can be avoided if the width of the pulse at the 1% level (FW1%M) is less than 430 ns.

Conventional pulse shaping filters, which use cascaded real poles, produce an asymmetric quasi-Gaussian pulse which becomes more symmetric as the filter order is increased. By using a pulse shaper with complex poles, more symmetric pulses can be obtained with a lower filter order. Hence, we can obtain lower series noise for the same filter order, or lower number of filter stages (thus lower power consumption) for the same noise. A bipolar pulse shape was selected, as its ability to reject low frequency noise, drift, and ion tails was deemed to compensate for the small increase in series noise.

### 2.2 Signal to Noise

In an interpolating system the fractional position resolution is related to signal to noise ratio (SNR) as

$$\sigma_x/x = k \sigma_Q/Q$$

where  $\sigma_x/x$  is the position resolution as a fraction of the interstrip spacing,  $Q/\sigma_Q$  is the signal to equivalent noise charge ratio, and  $k$  is a constant of order 1. To achieve the desired fractional resolution of 1% the SNR must be of order 200. The ionization produced in these chambers by a normal incidence track is 90 ion pairs, leading to an induced charge signal on the cathode strip of around 70 fC. Hence to achieve the desired position resolution all sources of electronic noise must amount to less than about 2500 r.m.s. electrons.

## 3. ELECTRONICS ORGANIZATION

Each chamber has eight 96-channel Amplifier-Storage Module (ASM) boards mounted around the chamber periphery. These boards pick up the 768 x-strips from the four precision cathode planes. The charge signals are

amplified and filtered by preamp/shaper (P/S) ASICs (12 channels per chip) and the amplified pulses are then sampled and stored in the SCA. The ASM board contains eight P/S, SCA, and ADC chips, along with control logic in a 12 x 24 x 0.5 cm volume. The raw data from the

ASM at a rate of about 1 Gbit/s is sent to the data concentrator on LVDS links.

A possible layout of the ASM board is shown in Figure 1.

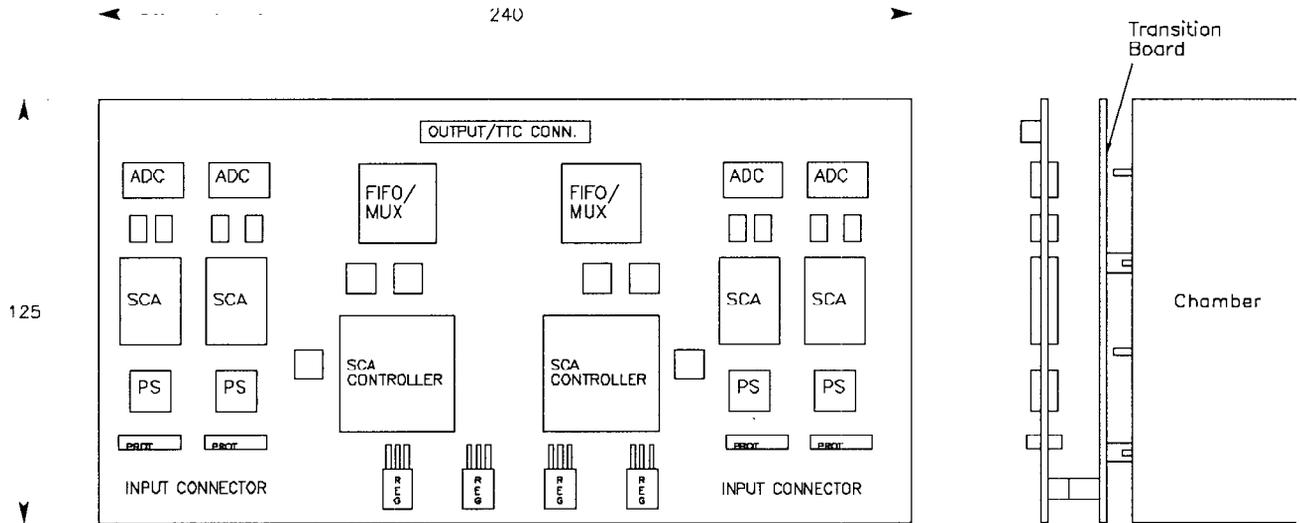


Figure 1

Figure 2 shows a diagram of the ASM board mounting on the chambers.

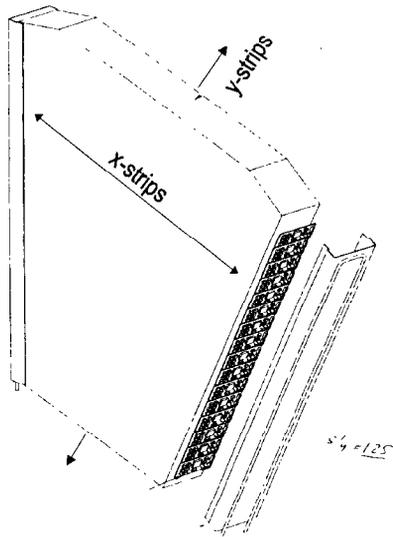


Figure 2

In Figure 3, the organization of the readout of one endcap is shown.

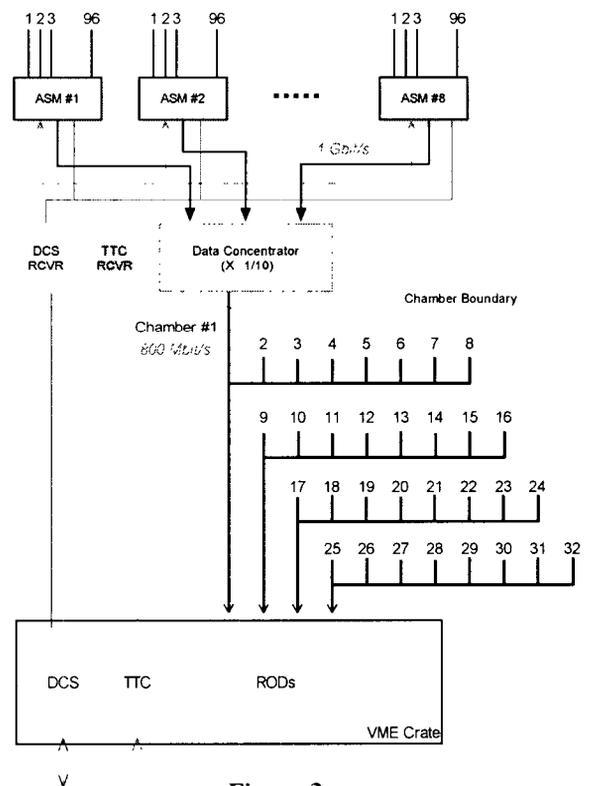


Figure 3

## 4. PREAMP/SHAPER ASIC

### 4.1 Preamp input transistor optimization

The input device is chosen to be an NMOS transistor with minimum channel length. Then, the width is selected to give minimum noise for the allotted power budget. Using the standard analysis the device width that minimizes series white noise is the one that gives a FET capacitance of  $CD_{et}/3$ . However, with  $0.5\mu\text{m}$  CMOS and input capacitance of  $50\text{ pF}$  the device would be biased in the weak inversion region where the standard analysis is no longer valid. We reduce the device width to put it near the border of weak-strong inversion to achieve a lower capacitance at the same gm. Finally, a behavioral model in MathCAD is used to select the input device dimensions. The current source and cascode devices in the preamp are also chosen for low noise using this mode.

### 4.2 DC feedback and compensation

For our expected strip capacitance of  $20 - 50\text{ pF}$  we choose a preamplifier feedback capacitance of  $1.2\text{ pF}$ . A NMOS FET biased in the triode region is used for DC feedback with an equivalent resistance of about  $1.2\text{ M}\Omega$ , which gives negligible parallel noise and keeps the reset time short enough to prevent the preamp from saturating under the highest expected rate. The bias is provided by a replica circuit which sets the feedback FET's gate potential with reference to the input/output potential of the amplifier; it is essential to use such a scheme which tracks temperature and process variation

to prevent excessive variation of the effective  $R_F$ .

The compensation circuit is a nonlinear version of the standard pole-zero compensation used in discrete designs. The compensation FET sees the same gate, source, and drain voltage as the feedback FET and so the two devices maintain a constant resistance ratio even as the preamp output swings in response to a large transient signal. In practice the feedback FET nonlinearity is well-compensated by this system.

### 4.3 Shaper

The method of Ohkawa [1] is used to design a 7th order shaper which is the best approximation to a true Gaussian waveform. The shaper has a single real pole and three second-order sections in cascade. Each second-order section is made with a multiple feedback topology. This arrangement uses a high-gain inverting amplifier whose input serves as a virtual ground, and has low sensitivity to component tolerances.

The amplifier stages used in the shaper are NMOS-input folded cascodes with a gain-bandwidth product of about  $200\text{ MHz}$ . The amplifiers dissipate about  $3\text{ mW}$  each. Small current sources at the inputs of each amplifiers allow the input and output DC levels to differ, where necessary to maintain high dynamic range.

The final stage is a symmetric OTA with rail-to-rail class AB output. Dissipating only  $5\text{ mW}$ , this circuit can drive up to  $400\text{ pF}$  capacitive loads to within  $0.1\text{ V}$  of either supply rail at slew rates of over  $50\text{ V}/\mu\text{sec}$ .

A block diagram of the P/S is shown in Figure 4.

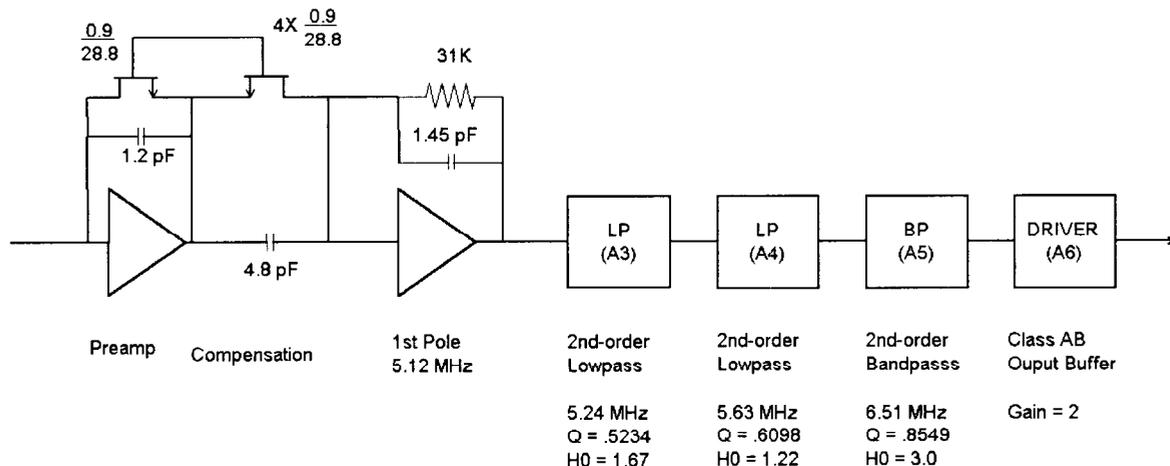


Figure 4

## 5. SCA

The SCA developed for the ATLAS Liquid Argon calorimeter [2] is well-suited for use in the CSC system. It is organized as 4 groups of (3 + 1 reference) channels, and is capable of simultaneous read and write at 40 MHz with 12 bit resolution. The readout logic of the LAr SCA is internally set to multiplex the outputs of two chips into a single ADC; a modification to the IC has been implemented to allow each SCA to be read out into its own ADC for higher throughput. Otherwise the architecture and pinout of the chip is unchanged.

## 6. P/S RESULTS

The first prototype of the CSC P/S was received from the foundry in early September 1999 and was found to function in very close agreement to simulations. Figure 5 shows the simulated (solid line) and measured (dotted) waveforms.

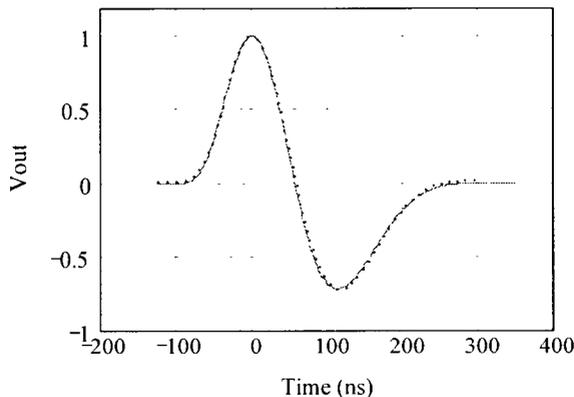


Figure 5

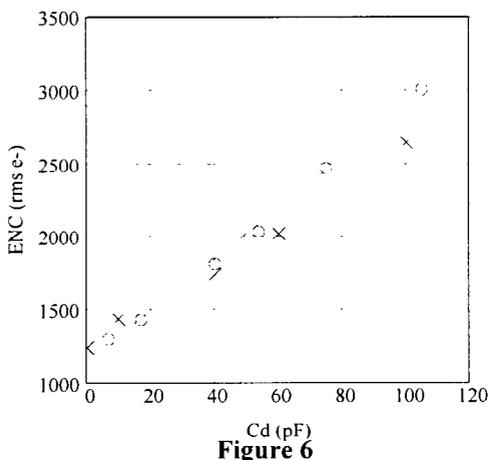


Figure 6

Noise and linearity results are shown in Figure 6 and Figure 7 respectively.

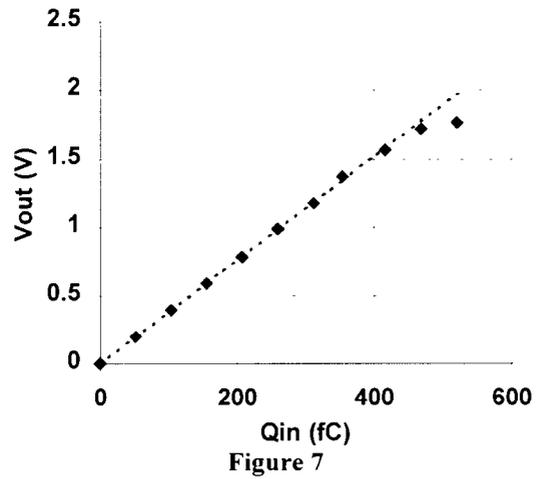


Figure 7

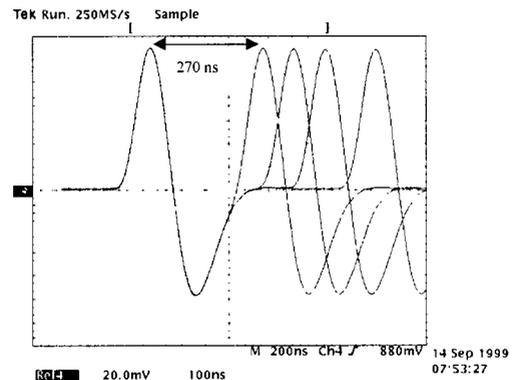


Figure 8

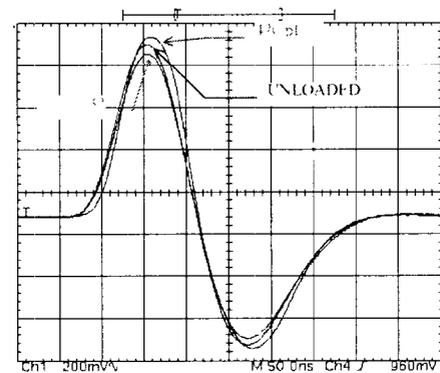


Figure 9

To simulate the effect of high rates, double-pulse signals at varying separations were injected. As shown in Figure 8, the interpulse spacing can be below 300 nsec without any pileup.

The Class AB output driver was able to drive low impedance loads with low distortion. Figure 9 shows the output waveform of the P/S unloaded, and loaded by 470 pF and 100 .

The performance of the P/S chip is summarized in Table I.

**Table I**

Technology	0.5 $\mu$ m CMOS
Channels	16
Die size	2.78 x 3.96 mm
Architecture	Single-ended
Intended Cdet	20 – 100 pF
Input device	NMOS W/L = 5000/0.6 $\mu$ m, Id = 4mA
Noise	1140 + 17.6 e-/pF
Gain	3.8 mV/fC
Max. linear charge	450 fC
Class AB Output swing	To power supply - 250 mV
Pulse shape	7 <sup>th</sup> order complex Gaussian, bipolar
Pulse peaking time, 5% - 100%	73 ns
FW1%M	340 ns
Max. output loading (3% distortion)	500 $\Omega$ , 500 pF
Crosstalk	0.8% adjacent, 0.5% non-adjacent channel
Power supply	Single +3.3V
Power Dissipation	32.5 mW/chan

## 7. Conclusions and Future Work

The front end electronics of the ATLAS CSC system is in development. The custom ASICs, typically the longest lead-time items in such a project, have completed one prototyping cycle and perform in accordance with specifications. Future efforts in design will concentrate on data selection/compression algorithms, controller hardware design, mechanics, interconnect, and cooling of the on-chamber components, and design of the fiber links and RODs. The first performance test of a complete front end prototype chain will take place this year in a test beam with high background simulation. Qualification testing for radiation tolerance, both of the custom and COTs components, will begin in 2000. Production is slated for 2001 - 2003.

## REFERENCES

[1] Ohkawa, NIM 138 (1976) 85-92, "Direct Syntheses of the Gaussian Filter for Nuclear Pulse Amplifiers"

[2] ATLAS Liquid Argon Calorimeter Technical Design Report, Dec. 16, 1996